vertically between layers. The various contact points can, for instance, be created within the surface of a power plane or ground plane 36. The layers within the interconnecting metalization structure of the present invention can contain signal interconnections in the X-direction, signal interconnections in the Y-direction, signal interconnections between X and or Y directions, interconnections to and/or within power and/or ground buses. The present invention further teaches the interconnection of signal lines, power and ground buses between the connected IC's and the top of the metalization system of the present invention.

Fig. 3a shows signal lines formed in the X-direction, Fig. 3b shows signal lines formed in the Y-direction.

Fig. 4 presents yet another application of the present invention. Shown in Fig. 4 is an exploded view of a part of Fig. 5 that presents an area array I/O distribution. Fig. 4 shows pads 41 (on which solder bumps can be created) and an example of a layout of the redistribution of the peripheral pads 41'. The exploded view of Fig. 4 is taken along the line 2-2' shown in Fig. 5, the redistribution of the peripheral pads 41' (see Fig. 4) is, for clarity of overview, not shown in Fig. 5. The power or ground connections can be made to any point that is required on

the bottom device. Furthermore, the power and ground planes can be connected to the power and ground planes of the package substrates. Fig. 4 shows an example of how to use the topmost metal layer to redistribute the peripheral pads 41′ to become area array pads 41. The solder bumps can then be created on pads 41.

Fig. 5 shows the top surface of a plane that contains a design pattern of a combination of power or ground pads 52 and signal pads 54. Fig. 5 shows the pad openings in the top dielectric layer. It is to be noted that the ground/power pads 52 are heavier and larger in design relative to the signal pads 54. The present invention ideally lends itself to meeting these differences in design, as they are required within the art of chip and high performance circuit design. The number of power or ground pads 52 shown in Fig. 5 can be reduced is there are power and/or ground planes within the chip. From this it is clear that the package number of I/O′s can be reduced within the scope of the present invention which leads to a reduction of the package cost by eliminating common signal/power/ground connections within the package. For instance, a 470 I/O count on a BGA chip can, within the scope of the present invention, be reduced

to a 256 I/O count using the present invention. This results in considerable savings for the overall package.

Fig. 6 shows a basic design advantage of the invention. This advantage allows for the sub-micron or fine-lines, that run in the immediate vicinity of the metal layers 3 and the contact points 6, to be extended in an upward direction 20 through metal interconnect 7′, this extension continues in the direction 22 in the horizontal plane of the metal interconnect 26 and comes back down in the downward direction 24 through metal interconnect 7″. The functions and constructs of the passivation layer 4 and the insulating layer 5 remain as previously highlighted under Fig. 1. This basic design advantage of the invention is to "elevate" or "fan-out" the fine-line interconnects and to remove these interconnects from the micro and sub-micro level to a metal interconnect level that has considerably larger dimensions and is therefore with smaller resistance and capacitance and is easier and more cost effectively to manufacture. This aspect of the invention does not include any aspect of conducting line re-distribution and therefore has an inherent quality of simplicity. It therefore further adds to the importance of the invention in that it makes micro and sub-micro wiring accessible at a wide-metal level. The interconnections 7′ and 7″ interconnect the fine-level metal by going up through the